CLAIMS

What is claimed is:

1. A microcontroller, which addresses program memory separately from data memory, the microcontroller comprising:

a CPU;

a boot memory coupled to the CPU;

a control coupled to the CPU and to the boot memory, which

in a first state causes the boot memory to be configured as data memory; and

in a second state causes the boot memory to be configured as program memory.

2. The microcontroller of claim 1 where the control includes

a memory control register, the memory control register comprising

a program enable flag, which

when it has a first value causes the control to be in the first state; and

when it has a second value causes the control to be in the second state.

3. The microcontroller of claim 1, further comprising

an external port coupled to the CPU and to the control; where

the external port is configured as a system bus when (1) the control is in the first state, and (2) the control is in the second state and the CPU is accessing an external memory as data memory; and

the external port is configured as an input/output port when the control is in the second state and the CPU is not accessing the external memory as program or data memory.

4. The microcontroller of claim 1, further comprising

an external port coupled to the control; where

the external port is configured as a system bus when the boot memory is addressed as data memory; and

the external port is configured as an input/output port when the boot memory is addressed as program memory.

5. The microcontroller of claim 1, further comprising

an external port coupled to the control; where

the external port is configured as a system bus when the boot memory is addressed as data memory and when the CPU writes to an external memory via the external port using an instruction that allows writes to program memory; and

otherwise, the external port is configured as an input/output port.

6. A microcontroller, which addresses program memory separately from data memory, the microcontroller comprising:

a control, having a first state and a second state;

a boot memory coupled to the control;

an external port coupled to the control; where

the external port is configured as a system bus when (1) the control is in the first state and the boot memory is not addressed, or (2) the control is in the second state and the external port is used to address an external memory as program or data memory; and

the external port is configured as an input/output port when the control is in the second state, the boot memory is addressed, and the external port is not used to address the external memory as data memory.

7. The microcontroller of claim 6 where

the boot memory is configured as data memory if the port control is in the first state; and

the boot memory is configured as program memory if the port control is in the second state.

8. The microcontroller of claim 6 where

the external port is configured as a system bus when the CPU writes to an external memory via the external port using an instruction that allows writes to program memory.

9. A method for loading a boot memory onboard a microcontroller, the microcontroller addressing program memory separately from data memory, the method comprising

configuring the boot memory to be addressed as data memory unless it is already configured to be addressed as data memory;

loading a program from an external program memory into the boot memory;

configuring the boot memory to be addressed as a program memory; and

executing the program in the boot memory.

10. The method of claim 9 where loading the program from the external program memory into the boot memory comprises

moving a word of the program from external program memory into a working register by directly addressing the working register; and

moving the word from the working register to a boot memory location by directly addressing the boot memory location as a register.

11. The method of claim 9 where the boot memory is divided into banks, the boot memory is addressable using offset addressing within the banks, and loading the program from the external program memory into the boot memory comprises

moving a word of the program from external program memory into a working register by directly addressing the working register; and

moving the word from the working register to the boot memory by offset addressing the boot memory.

12. The method of claim 9 where configuring the boot memory to be addressed as data memory includes

setting the state of a control flag.

13. The apparatus of claim 12 where setting the state of the control flag comprises

setting a bit in a memory control register.

14. An apparatus for booting a microcontroller, which addresses program memory separately from data memory, by loading a program from an external program memory into a boot memory on the microcontroller, the apparatus comprising

a control coupled to the boot memory, which in a first state causes the microcontroller to address the boot memory as data memory, and in a second state causes the microcontroller to address the boot memory as program memory; and

a first program stored in the external program memory which causes the microcontroller to

switch the control to the first state;

transfer a second program from the external program memory to the boot memory;

switch the control to the second state; and

execute the second program in the boot memory.

15. The apparatus of claim 14 further comprising

an external port coupled to the control, which operates as a system bus when (1) the control is in the first state, or (2) the control is in the second state and the CPU is accessing the external program memory as program or data memory, and which operates as an input/output port when the control is in the second state and the CPU is not accessing the external program memory as program or data memory.

16. The apparatus of claim 15 where

the first program causes the microcontroller to transfer the second program from the external program memory to the boot memory via the external port; and

the second program causes the microcontroller to use the external port as an input/output port and as a system bus.

17. A method for using a microcontroller, which addresses program memory separately from data memory and which includes a boot memory, to debug software stored in an external memory, the method comprising

repeating the following until the debug process is complete:

loading communication software into the boot memory;

loading a bootloader into the boot memory;

executing the communication software and the bootloader;

modifying the software stored in the external memory through the communications software and the bootloader;

loading debug software into the boot memory;

executing the debug software and the communication software;

executing the software stored in the external memory; and

stopping execution of the software stored in the external memory.

18. The method of claim 17 where loading communication software into the boot memory includes

converting the boot memory so that it is addressed by the microcontroller as data memory unless the boot memory is already addressed as data memory;

loading the communication software into the boot memory; and

converting the boot memory so that it is addressed by the microcontroller as program memory.

19. A microcontroller, comprising

a CPU;

program address and data busses coupled to the CPU;

data address and data busses coupled to the CPU;

input/output busses coupled to the CPU;

an onboard RAM comprising a boot RAM;

a memory selector, coupled to the program address and data busses, the data address and data busses and the boot RAM, which can be actuated to select whether the boot RAM is addressed by the program address and data busses or the data address and data busses;

an external interface;

an output port selector, coupled to the program address and data busses, the input/output busses and the external interface, which can be actuated to select the program address and data busses or the input/output busses to couple to the external interface;

a memory control coupled to the CPU for actuating the memory selector; and

an output port control coupled to the CPU for actuating the output port selector.